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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/624,483	07/23/2003	Hidehiro Shiga	240575US2S	7443

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/624,483	SHIGA ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) *3* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☒ Claim(s) *4-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 02/02/2004 is acceptable.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Election/ Restriction

3. Applicant's election without traverse of Species I, **claims 1-2 and 4-10**, in the reply filed on 04/20/2006 is acknowledged.

4. Claim 3 is withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 04/20/2006, as noted above.

Drawings

5. Figures 8-9 and 11 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header

(as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

6. **Claim 1** is objected to because of the following informalities: Claim 1 recites: "a second impurity diffusion layer formed on the surface of the semiconductor substrate in a state of being separated from the first impurity diffusion layer of an end of the first impurity diffusion layers, having a second area, and constituting a source/drain diffusion layer of the cell transistor" and "a second gate electrode provided on the semiconductor substrate with a gate insulating film interposed therebetween between the first impurity diffusion layer of the end and the second impurity diffusion layer along a second direction, and constituting a gate of the select transistor", wherein the limitation "a second impurity diffusion layer formed on the surface of the semiconductor substrate in a state of being separated from the first impurity diffusion layer of an end of the first impurity diffusion layers, having a second area, and constituting a source/drain diffusion layer of the cell transistor" should be "a second impurity diffusion layer formed on the surface of the semiconductor substrate in a state of being separated from the first impurity diffusion layer of an end of the first impurity diffusion layers, having a second area, and constituting a source/drain diffusion layer of the **select** transistor" because this should-be limitation is most consistent with the specification and the drawings, and such is interpreted for examination.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. **Claims 1-2** are rejected under 35 U.S.C. 102(b) as being anticipated by Dehm et al. U.S. Patent Application Publication 20020123203 (the '203 reference).

The '203 reference discloses in the figures, particularly Figs. 3-4, and respective portions of the specification a semiconductor memory device as claimed.

Referring to **claim 1**, the reference discloses a semiconductor memory device, which includes:

a cell block (Fig. 4a) composed of several series-connected units (one unit depicted in Fig. 3) having a ferroelectric capacitor (C_{ferro}) and a cell transistor (no label) parallel-connected to the ferroelectric capacitor; and

a select transistor (generally indicated at BS, Fig. 3) connected to an end of the cell block, the semiconductor memory device comprising:

a semiconductor substrate (no number, best seen in Fig. 4b);

a plurality of first impurity diffusion layers (no number, best seen in Fig. 4a, with the aid of Fig. 4b and Fig. 3) formed on the surface of the semiconductor substrate in a state of being mutually separated along a first direction, having a first area, and constituting a source/drain diffusion layer of the cell transistor;

a second impurity diffusion layer (no number, best visualized in Fig. 3) formed on the surface of the semiconductor substrate in a state of being separated from the first impurity diffusion layer of an end of the first impurity diffusion layers, having a second area, and constituting a source/drain diffusion layer of the select transistor;

a plurality of first gate electrodes (generally indicated at 7, Fig. 4b, and at WLn, wherein n is an integer, Fig. 3) provided on the semiconductor substrate with a gate insulating film (no number) interposed therebetween between the first impurity diffusion layers along a second direction, and constituting a gate of the cell transistor;

a second gate electrode (generally indicated at BS, Fig. 3) provided on the semiconductor substrate with a gate insulating film (no number) interposed therebetween between the first impurity diffusion layer of the end and the second impurity diffusion layer along a second direction, and constituting a gate of the select transistor; and

a contact (not shown) electrically connecting a bit line (BL) and the second impurity diffusion layer (paragraph [0005]).

Referring to **claim 2**, the reference further discloses a plurality of ferroelectric capacitors having both terminals (generally indicated at 2 and 3, Fig. 4b) connected to the first impurity diffusion layers on both sides of the first gate electrode, and having a ferroelectric film (no

number), and first and second electrodes (generally indicated at 2 and 3/4, Fig. 4b) sandwiching the ferroelectric film.

8. **Claims 1-2** are rejected under 35 U.S.C. 102(b) as being anticipated by Takashima U.S. Patent Application Publication 20020027798 (the '798 reference).

The '798 reference discloses in the figures, particularly Figs. 6-7 and 167, and respective portions of the specification a semiconductor memory device as claimed.

Referring to **claim 1**, the reference discloses a semiconductor memory device, which includes:

a cell block (Figs. 6's) composed of several series-connected units (one unit depicted in the figures) having a ferroelectric capacitor (Cn, wherein n is an integer) and a cell transistor (Qn, wherein n is an integer) parallel-connected to the ferroelectric capacitor; and

a select transistor (generally indicated at BS0, Figs. 6 and 7) connected to an end of the cell block, the semiconductor memory device comprising:

a semiconductor substrate (no number, best seen in Fig. 7B);

a plurality of first impurity diffusion layers (no number, generally indicated at n+, Figs. 7A and 7B) formed on the surface of the semiconductor substrate in a state of being mutually separated along a first direction, having a first area, and constituting a source/drain diffusion layer of the cell transistor;

a second impurity diffusion layer (no number, generally indicated at n+, Figs. 7A and 7B) formed on the surface of the semiconductor substrate in a state of being separated from the first

impurity diffusion layer of an end of the first impurity diffusion layers, having a second area, and constituting a source/drain diffusion layer of the select transistor (BS0);

a plurality of first gate electrodes (WL0n, wherein n is an integer, Figs. 7's) provided on the semiconductor substrate with a gate insulating film (no number) interposed therebetween between the first impurity diffusion layers along a second direction, and constituting a gate of the cell transistor;

a second gate electrode (BS0) provided on the semiconductor substrate with a gate insulating film (no number) interposed therebetween between the first impurity diffusion layer of the end and the second impurity diffusion layer along a second direction, and constituting a gate of the select transistor; and

a contact (no number) electrically connecting a bit line (BL) and the second impurity diffusion layer.

Referring to **claim 2**, the reference further discloses a plurality of ferroelectric capacitors having both terminals (generally indicated at lower electrode and upper electrode, Figs. 167's) connected to the first impurity diffusion layers on both sides of the first gate electrode, and having a ferroelectric film (no number), and first and second electrodes (lower electrode and upper electrode) sandwiching the ferroelectric film.

Allowable Subject Matter

9. Claim 4 and dependent-upon-claim-4 claims 5-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a semiconductor memory device having all limitations as recited in claim 4 having said third length and said fourth length as claimed.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 7:30 am - 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
April 30, 2006